

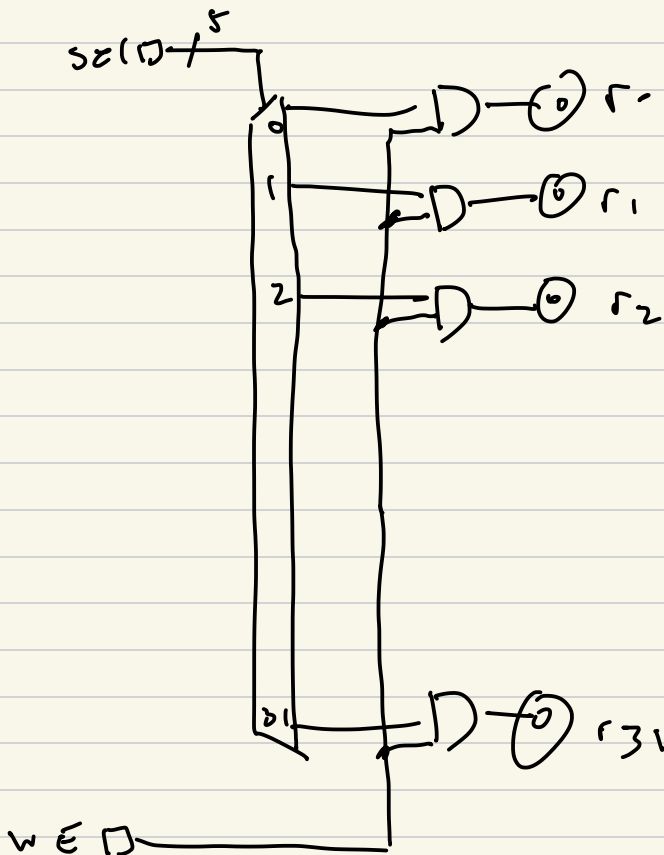
CS 315-01 Lab Processor ALU 2025-10-29

add rd to, ^{rs1} t', ^{rs2} t2 RD0 + RD1

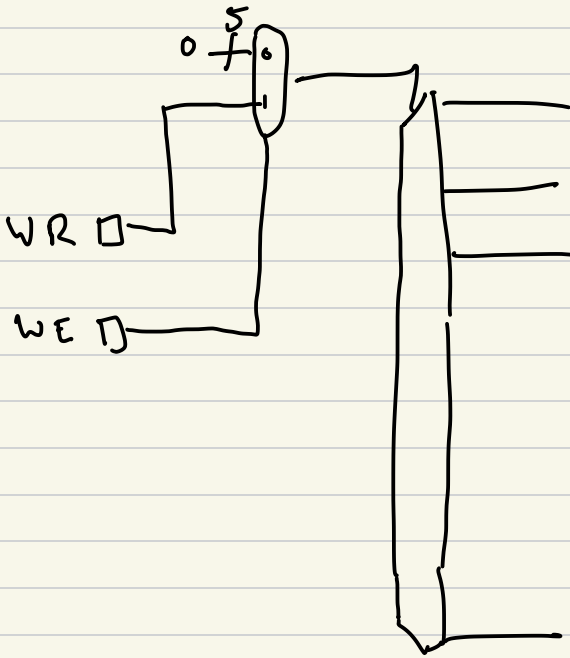
 ↗ ↓ ↓

 WR RR0 RR1

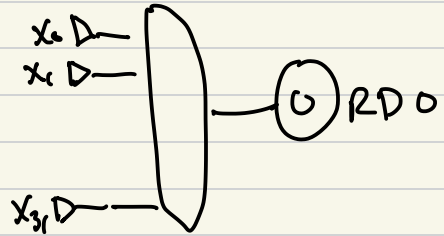
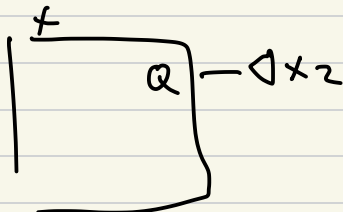
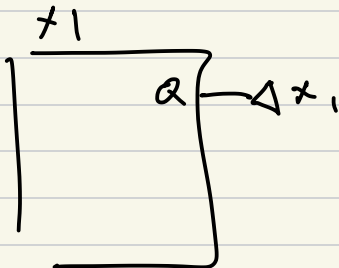
Decoder with Enable



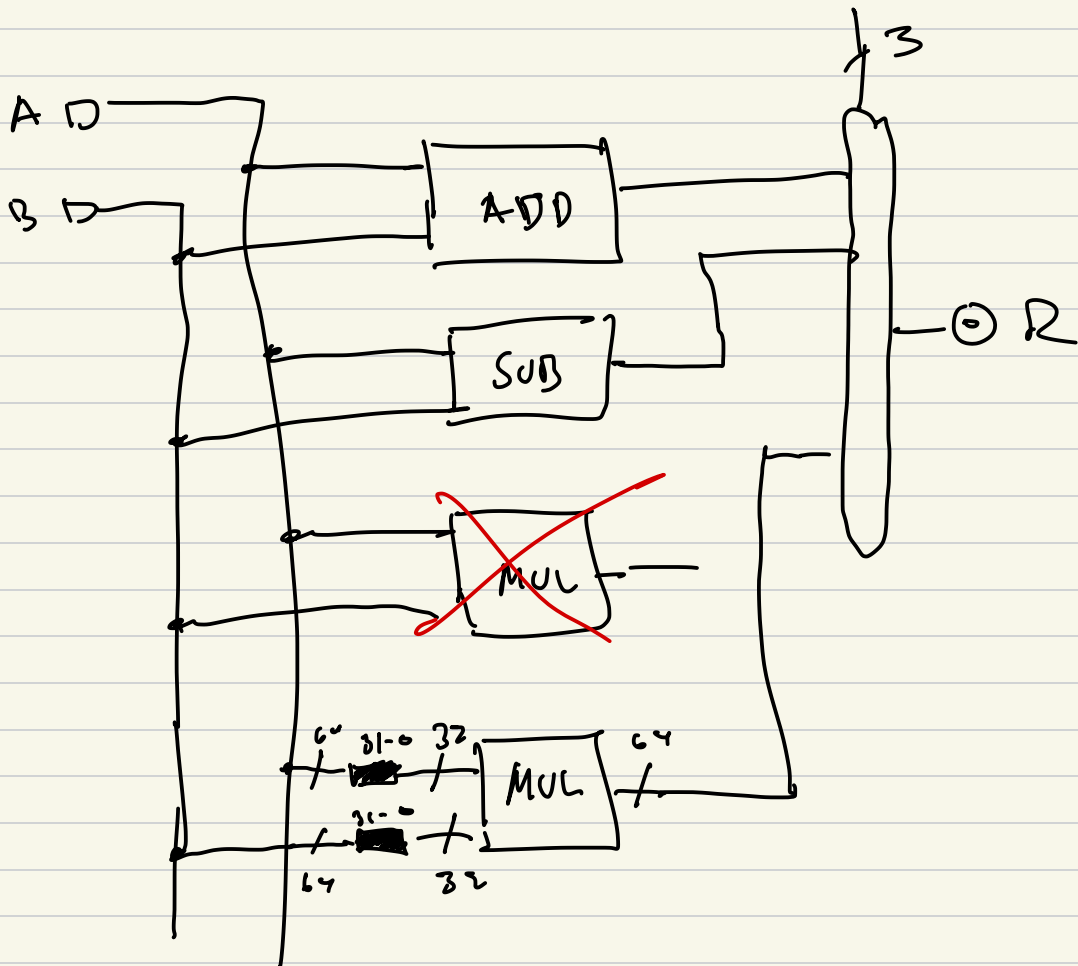
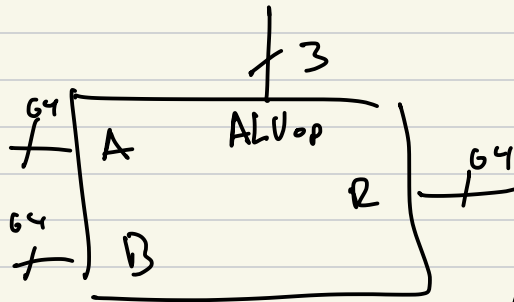
Alt Approach



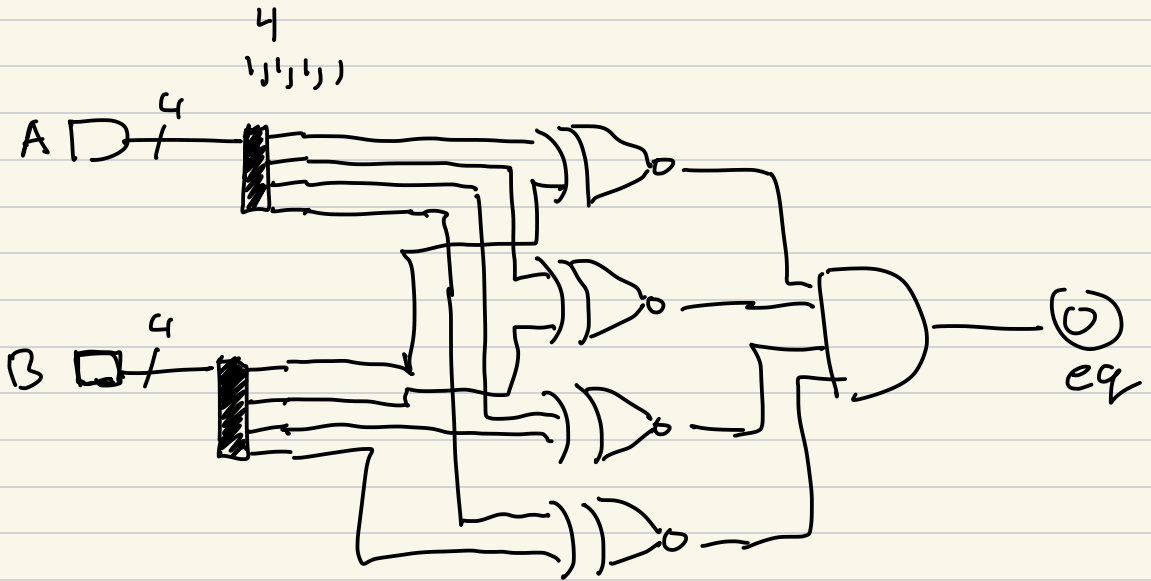
$x_0 \rightarrow \Delta x_0$



ALU Arithmetic Logic Unit



4-bit Comparator



a	b	x_{eq}	x_{neq}
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1